Novel Fabrication Method for Studying Electron Transport in Nanometer-sized Devices

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Introduction

Nano-fabrication is an essential aspect for studying the properties of nanometer-sized materials. In the semiconducting industry, it is a process used to create integrated circuits that are present in everyday electronic devices. In this project, a fabrication method is developed to study the electronic transport properties of novel condensed matter systems such as single crystal nanowires and nanobeams. Steps include dispersion, sample identification, designing and drawing contact patterns, and metallization. Each step will be presented here together with measurements resulting from this method.

Dispersion

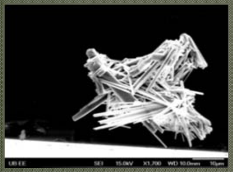

Fig. 1a
SEM image of a cluster of single-crystal W-doped VO_2 nanowires

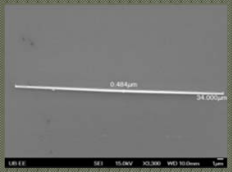

Fig. 1b
SEM image of a single W-doped VO_2 nanowire after dispersion

Nanowires were synthesized by methods described elsewhere [4]. Before dispersion the wires are bunched together in clumps (Fig 1a). To isolate them individually the clumps are submerged in isopropanol, (~20 mL). Then a few minutes of ultrasonication is used to break up the clumps even further. This dilute solution is then extracted with a syringe and sprayed onto a Si/SiO_2 substrate. This results in single nanowires left on the surface.

Identification

The location of wires on the substrate are identified under optical microscope relative to pre-defined position markers (Fig 2). Choice of samples is based not only on location, but also on length, thickness, and uniformity.

Fig. 2. Optical image of W-doped nanowire. The position marker in the bottom right corner indicates the row, column, and grid number. Scale bar = 5 μm.

Designing, Drawing and Metallization

After identification, electrical contact patterns are designed using a software, namely AutoCAD. (Fig. 3a).

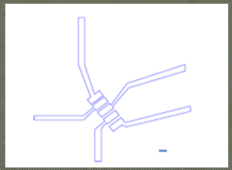

Fig. 3a
Design of fingers, which are electrical contacts to the sample. Scale bar = 3 μm.

Fig. 3b.
Optical image of device after metallization. Contacts are Cr/Au (5nm/75nm). Scale bar = 3 μm.

The AutoCAD designs will then be uploaded into Nanometer Pattern Generation System (NPGS) program, which communicates with the electron beam lithography (EBL) set-up inside an SEM to write the pattern. After coating the sample with an electron-sensitive polymer known as PMMA, EBL uses a beam of electrons to etch the pattern into the PMMA. EBL has the capability of resolving patterns down to ~ 10 nm. Electron beam evaporation of Ohmic material (typically gold) provides the metallization and final step in the process (Fig 3b).

Measurements

In W-doped VO_2 we observe a voltage-driven metal-insulator transition [1] (Fig 4a). For Sb_2Te_3, which is a topological insulator (TI), we apply a gate voltage to tune the carrier density in the sample (Fig 4b). TI is a novel material which supports carrier transport on its surface, but is insulating inside the bulk [2].

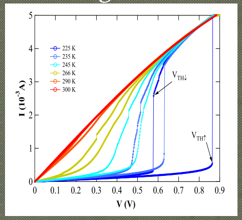

Fig. 4a.
Current vs voltage of single crystal W-doped VO_2 nanowire [3].

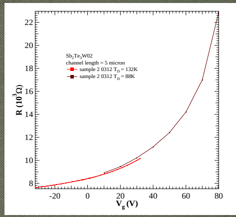

Fig. 4b.
Resistance vs gate voltage of single crystal Sb_2Te_3 nanowire.

References

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